Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A semiconductor device, comprising:
at least one structure, each said structure comprising an input island, a processing island, and an output island formed within the semiconductor device, said input island is adapted to accept a specified amount of data, said input island is further adapted to enable a means for providing a first specified voltage for powering the processing island after accepting the specified amount of data, said processing island is adapted to receive and process the specified amount of data from the input island upon said powering by the first specified voltage, said output island is adapted to be powered by a second specified voltage, said processing island is further adapted to transmit the processed data to the output island upon said powering by the second specified voltage, and said first specified voltage is adapted to be disabled thereby removing power from processing island upon completion of transmission of the processed data to the output island.

[c2] The semiconductor device of claim 1, wherein the input island comprises a first memory device for collecting the

specified amount of data and a control device for enabling and disabling the first specified voltage, controlling a flow of the specified data to the processing island, enabling and disabling the second specified voltage, and controlling the transmission of the processed data to the output island, and wherein the output island comprises a second memory device for collecting the processed data from the processing island.

[c3] The semiconductor device of claim 2, wherein the first memory device and the second memory device are buffers.

[c4] The semiconductor device of claim 2, wherein the first memory device and the second memory device are selected from the group consisting of first in-first out (FIFO) memory and last in-first out (LIFO) memory.

[c5] The semiconductor device of claim 1, wherein the first specified voltage is not equal to the second specified voltage.

[c6] The semiconductor device of claim 1, further comprising a third specified voltage for powering the input device, wherein the first specified voltage, the second specified voltage, and the third specified voltage are not equal to a same voltage.

[c7] The semiconductor device of claim 1, wherein the at least one structure comprises a plurality of said structures, wherein each of said structures comprise means for communicating and transferring data between each of said structures.

[c8] The semiconductor device of claim 1, further comprising means for prioritizing the specified amount of data in the input island for a specified order of transmission to the processing island.

[c9] A semiconductor device, comprising:
a plurality of memory islands, a plurality of processing islands, and a control island formed within the semiconductor device, said memory islands are adapted to accept a specified amount of data, said processing islands are adapted to receive and process the specified amount of data from each of said memory islands, said memory islands are further adapted to accept the processed data from each of said processing islands, said control island is adapted to supervise and control data transfer between said memory islands and said processing islands, said control island comprises means for enabling and disabling a plurality of voltages for powering each of said memory islands and each of said processing islands.

[c10] The semiconductor device of claim 9, wherein each of said of said memory islands are adapted to be powered only while performing a memory function, and wherein each of said processing islands are adapted to be powered only while performing a processing function.

[c11] The semiconductor device of claim 9, each of the plurality of voltages are not a same voltage.

[c12] The semiconductor device of claim 9, wherein the plurality of memory islands are buffers.

[c13] The semiconductor device of claim 9, wherein the plurality of memory islands are selected from the group consisting of first in-first out (FIFO) memory and last in-first out (LIFO) memory.

[c14] The semiconductor device of claim 9, further comprising means for prioritizing the specified amount of data in each of the plurality of memory islands for a specified order of transmission to each of the processing islands.

[c15] 15. A method, comprising:
providing a structure comprising an input island, a processing island, and an output island formed within a semiconductor device;
collecting by the input island a specified amount of data;
enabling by the input island means for providing a first

specified voltage for powering the processing island after collecting the specified amount of data;
receiving by the processing island the specified amount of data from the input island upon said powering by the first specified voltage;
processing by the processing island the specified amount of data from the input island;
powering by a second specified voltage the output island;
transmitting by the processing island the processed data to the output island upon said powering by the second specified voltage; and
disabling the first specified voltage thereby removing power from processing island upon completion of transmission of the processed data to the output island.

[c16] The method of claim 15, wherein the input island comprises a first memory device and a control device, wherein the output island comprises a second memory device, and wherein the method further comprises;
collecting by the first memory device the specified amount of data;
enabling by the control device the means for providing the first specified voltage for powering the processing island after collecting the specified amount of data;
controlling by the control device a flow of the specified

data to the processing island;

processing by the processing island the specified amount of data from the input island;

enabling by the control device the second specified voltage for powering the second memory device;

controlling, by the control device the transmission of the processed data to the second memory device;

disabling by the control device the means for providing the first specified voltage for powering the processing device;

The method of claim 16, wherein the first memory device and the second memory device are buffers.

[c17] The method of claim 16, wherein the first memory device and the second memory device are buffers.

[c18] The method of claim 16, wherein the first memory device and the second memory device are selected from the group consisting of first in-first out (FIFO) memory and last in-first out (LIFO) memory.

[c19] The method of claim 15, wherein the first specified voltage is not equal to the second specified voltage.

[c20] The method of claim 15, further comprising powering by a third specified voltage the input device, wherein the first specified voltage, the second specified voltage, and

the third specified voltage are not equal to a same voltage.

[c21] The of method claim 15, further comprising a plurality of said structures, wherein each of said structures comprise means for communicating and transferring data among said structures.

[c22] The method of claim 15, further comprising prioritizing the specified amount of data in the input island for a specified order of transmission to the processing island.

[c23] A method, comprising:
providing a plurality of memory islands, a plurality of processing islands, and a control island formed within a semiconductor device;
collecting by each of said memory islands an individually specified amount of data;
receiving and processing by each of said processing islands the individually specified amount of data from each of said corresponding memory islands;
collecting by each of said memory islands the processed data from each of said corresponding processing islands;
controlling and supervising by the control island data transfer between each of said memory islands and each of said processing islands;
enabling and disabling by the control island a plurality of

voltages for powering each of said memory islands and each of said processing islands.

[c24] The method of claim 23, further comprising powering each of said memory islands and each of said processing islands only while performing a function.

[c25] The method of claim 23, wherein each of the plurality of voltages are not equal to each other.

[c26] The method of claim 23, wherein the plurality of memory islands are buffers.

[c27] The method of claim 23, wherein the plurality of memory islands are selected from the group consisting of first in-first out (FIFO) memory and last in-first out (LIFO) memory.

[c28] The method of claim 23, further comprising prioritizing the specified amount of data in each of the plurality of memory islands for a specified order of transmission to each of the corresponding processing islands.